IN THE CLAIMS:

1. – 7. (Canceled)

8. (Currently amended) A gate electrode, comprising:

a gate layer disposed above a substrate, said gate layer having a substantially level upper surface;

a conductive layer disposed over said gate layer, said conductive layer extending beyond edges of said gate layer;

thin first spacers disposed in contact with opposite sides of said gate layer and below said conductive layer; and

thick second spacers disposed in contact with said thin first spacers, each thick second spacer having a width which is constant in a direction parallel with said thin first spacers.

9. (Canceled)

10. (Previously presented) The gate electrode of claim 8, wherein said gate layer comprises polysilicon.

11. (Previously presented) The gate electrode of claim 10, wherein said conductive layer comprises polycide.

12. (Previously presented) The gate electrode of claim 8, wherein said thin first spacers comprise oxide.

13. (Canceled)

14. (Previously presented) The gate electrode of claim 11, wherein said polycide comprises titanium salicide (TiSi2).

15. - 122. (Canceled)

123. (Previously presented) The gate electrode of claim 8, wherein said thick second spacers comprise nitride.

124. (Previously presented) The gate electrode of claim 8, wherein the thin first spacers are at least as high as the thick second spacers.

Cmt G1

125. (Previously presented) The gate electrode of claim 8, wherein the thick second spacers are at least twice as thick as the thin first spacers.

126. (Previously presented) The gate electrode of claim 125, wherein the thick second spacers are between 300 and 2000 Å thick.

127. (Previously presented) The gate electrode of claim 126, wherein the thick second spacers are at least 800 Å thick.

128. (Previously presented) The gate electrode of claim 125, wherein the thick second spacers are at least 800/100 times as thick as the thin first spacers.